Flying Capacitor Multilevel Inverter Based Shunt Active Power Filter with Trifling Susceptibility to Divisional Voltages Deregulation

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Abstract— **Due to increasing utilization of shunt active power filter (APF) in power systems, necessarily it has to be effective and reliable as much as possible. In this paper to enjoy of multilevel inverter advantages in active filtering task, a shunt APF based on flying capacitor multilevel inverter is presented. The power section of this active filter is viewed as analog to digital converter; as a result a multilevel Sigma-Delta modulation control can be utilized to control power section of APF aimed at reducing sensitivity to flying capacitor voltage deregulation and improving modulator performance. In control section of this APF, perfect harmonic cancellation (PHC) method which is capable of correct action under any condition of use, is exploit. Simulation studies are performed using PSCAD/EMTDC® to validate proposed APF performance.**

Keywords-shunt active filter, flying capacitor inverter, perfect harmonic cancellation, power quality, Sigma-Delta,

I. INTRODUCTION

Due to the developments of semiconductor devices and microprocessor technology besides continuously reduction of them cost, shunt active power filters (APF) is going to play important role in reducing harmonic currents and reactive power in power lines. Therefore it is favorable to increase its effectiveness and reliability as much as possible.

As is shown in Fig. 1, Shunt active power filters generally consist of two distinct main blocks: a) the active filter controller b) The power converter. Controller is responsible for determining in real time the instantaneous compensating current references, which are continuously passed to the grid. The power converter is responsible for synthesizing the compensating current that should be drawn from the power system by utilizing a modulation method. It is quite clear that effectiveness and reliability of APF in compensating harmonic current sources can vary by changing three characteristics: a) The method implemented to generate the references b) The design characteristics of the converter, c) Modulation method used.

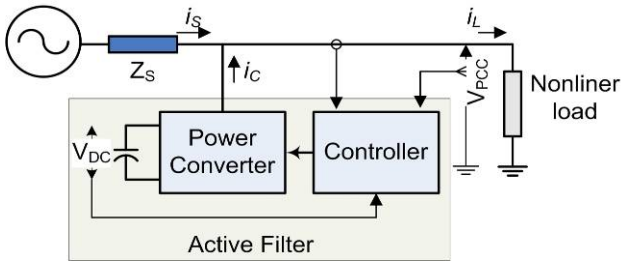

Figure 1. Block diagram of a shunt active power filter.

In this paper, it is tried to ameliorate APF performance by modifying these characteristics. In control section of proposed APF, perfect harmonic cancelling method (PHC) is used to generate reference currents because it has best performance among other control methods [1], [2].

The conventional APFs are designed based on simple two-level voltage source inverter (VSI) and use transformer to meet desired voltage profile [3], [4]. The transformer adds to the losses in the system and it may saturate once the load draws any DC current. Further at higher power, long tail current associated with the device characteristics prohibits high frequency operation and the efficiency of the APF is lower due to significant switching losses. Therefore, the APF control in high power applications faces difficulties. With respect that multilevel inverters can directly output high voltage without transformer and have high power conversion capability and furthermore achieve a high equivalent switching frequency effect at rather low device switching frequency [5]. In this work to address above mentioned problems, a flying capacitor multilevel inverter (FCMLI) benefits power section of APF. Besides, to reduce flying capacitor voltage deregulation and system nonlinearity on FCMLI performance, multilevel ΣΔ modulation concept applied to modulation control of FCMLI. As a result the advantages of this modulation appeared in communication literatures can be enjoyed.

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II. CONTROL STRATEGY

The operation principle of control section is to drive the harmonic and reactive component of the load current through harmonic and reactive detection circuit and reverse it as the reference compensating current. There is various control strategies presented in literatures [1]-[3]. One of these strategies is the PHC control strategy proposed by Rafiei et al., in 2001 [1]. It is the only strategy which can guarantee balanced, sinusoidal compensated currents, even when the system voltage at the point of common coupling (PCC) is itself already distorted and/or unbalanced therefore among various formal methods explained in literatures [1], PHC method is selected because of its advantages [1], [2].

In the PHC strategy the load active power is calculated as follow:

$$P(t) = i_a e_a + i_b e_b + i_c e_c = P_{dc} + P_{ac} \quad (1)$$

Then, only the fundamental components of the load voltages are considered for determining the desired currents. Therefore,

$$\begin{bmatrix} i_{S0} \\ i_{S\alpha} \\ i_{S\beta} \end{bmatrix} = \frac{P_{dc}}{(\bar{e}_\alpha)^2 + (\bar{e}_\beta)^2} \begin{bmatrix} 0 \\ \bar{e}_\alpha \\ \bar{e}_\beta \end{bmatrix} \quad (2)$$

$$i_{C-ref} = i_L - i_S \quad (3)$$

Where $\bar{e}_\alpha$ and $\bar{e}_\beta$ the fundamental components of the load voltages and can be obtained from the measured voltages by means of two simple band-pass filters Also, P_{dc} is filtered from $P(t)$ using a simple low-pass filter. Fig. 2 shows this control strategy block diagram.

Equation (3) is the mathematical representation of compensating current, and power converter is responsible for synthesizing it, that should be drawn from the power system.

III. POWER CONVERTER OF SHUNT ACTIVE POWER FILTER

To solve mentioned problem associated with two-level VSI based APFs, utilizing multilevel inverter is considered in this work. Main advantage of multilevel inverters is that they can reduce the displeasing harmonic content generated by the active filter itself because they can produce more levels of voltages than conventional inverters. Furthermore they can reduce the voltage or current ratings of the semiconductors, and hence expand the application of IGBTs and MOSFETs to the high power uses previously dominated by GTOs. Low switching losses compared with two-level inverter, low electromagnetic emission, higher flexibility and omitting problem of designing the costly and bulky snubber circuits are of the other merits of these inverters[5], [6].

At present, multilevel inverters are categorized into three groups [5]: i) diode clamped multilevel inverter (DCMLI) ii) cascade H-bridge inverter (CHBMI) and iii) flying capacitor multilevel inverter (FCMLI). DCMLI suffers from the limitations of DC link voltage unbalance, indirect clamping of the inner devices and multiple blocking voltages of the clamping diodes [5], [7]. CHBMI suffers from requirement of large number of converters to decrease harmonic and limited combination of switching patterns. Moreover for reactive power exchange, the power pulsation at twice the output frequency occurring with the DC link of H-bridge inverter necessitates oversizing of the DC link capacitors [8], [9]. Furthermore in shunt compensator applications a transformer is necessary to connect the cascade inverter structure to the distribution system, once a single DC link capacitor is used for all the three phases [9]. The FCMLI attempts to address some of the limitations imposed by the above mentioned inverters. The DC capacitor voltage regulation loop in FCMLI is independent of the number of output voltages levels and very simple. The use of capacitors for voltage clamping instead of diodes as in DCMLI, directly clamp the voltage across the switches unlike DCMLI, permits several switching combination for a particular voltage level generation, which may used for preferential charging and discharging of capacitor the method which is used in this paper [10]. A FCMLI is shown in Fig. 3.

With the increase in levels the synthesized output waveform approaches the reference signal with minimum distortion. Unfortunately the number of achievable voltage levels is limited due to complexity, voltage unbalance problem, voltage clamping requirements, circuit layout, cost and packaging constrains [6]. Hence to achieve the performance of high level inverter without any hardware modifying ΣΔ modulation control is utilized to control 5-level FCMLC.

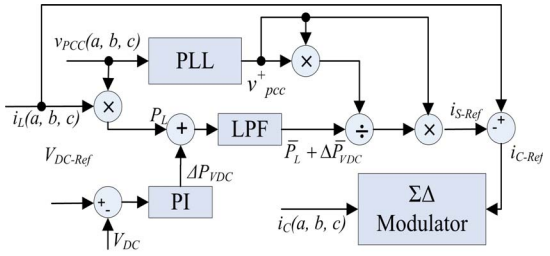

Figure 2. Control stage based on PHC strategy.

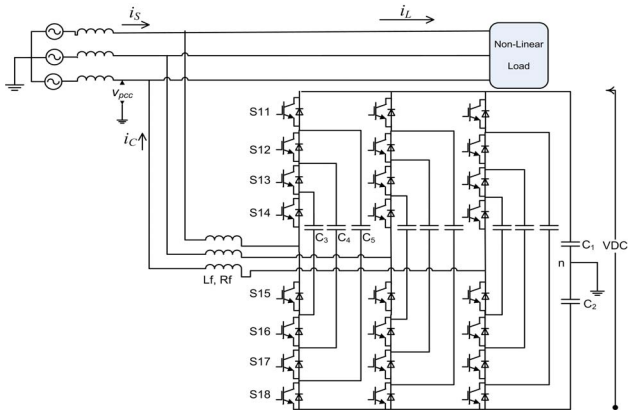

Figure 3. Schematic of power system and a FCMLI based shunt APF.

IV. ΣΔ MODULATION METHOD

In an N-level voltage source converter, the voltage of the DC-link is divided in to N-1 equal divisional voltages, each of which can be switched onto the load so that an N-level staircase like voltage waveform can be obtained. Such conversion scheme is similar to a multilevel digital converter (ADC). So power converter switching power converter can be regarded as multilevel ADC. The quantization process involved in A/D conversion is an inherently non-linear operation and introduces errors to the conversion [11]. In both communications and power electronics applications, the aim is to design the system so that the input signal is passed through the system with minimal distortion from noise. ΣΔ modulator is one of noise reduction methods [12]. ΣΔ modulators achieve the performance of high resolution quantizers by using low resolution quantizers in a feed-back loop with linear filtering. This structure is shown in Fig. 4.

This modulator do not reduce the magnitude of the quantization noise, but instead shape the power density spectrum of this error moving the energy towards high frequencies and reduce quantization noise within the signal band (Fig. 5). Increased noise in the high frequency band can easily remove by using simple low pass filter because noise frequency and fundamental frequency are separate. Since power switching converters typically switch at frequencies well in excess of the Nyquist rate of the reference signal, ΣΔ modulation technique can be extended and employed to synthesize a multilevel waveform by replacing the binary quantizer with a N-level quantizer corresponding to the number of levels of the multilevel inverter [13]. Second-order ΣΔ modulator is a better compromise between circuit complexity and signal to noise ratio [14]. Therefore this modulator is chosen for emerging in proposed APF.

Using an FCMI as an APF lies in obtaining fast and accurate performance in harmonic compensation whilst maintaining the voltage across the floating capacitors at the appropriate constant level. Large capacitor voltage swings may cause voltage stress across devices, consequently poor harmonic control performance and even inverter failure. Hence to address the divisional voltage deregulation, the power stage of converter can be embedded in the ΣΔ loop.

Here the multilevel quantizer, multilevel interface logic (MLIL) and multilevel VSI forms the quantizer, thus the divisional voltage deregulation is part of the quantization noise and will be attenuated by ΣΔ loop. With inverter embedded in the ΣΔ modulation loop, ΣΔ modulation control is insensitive to divisional voltage deregulation.

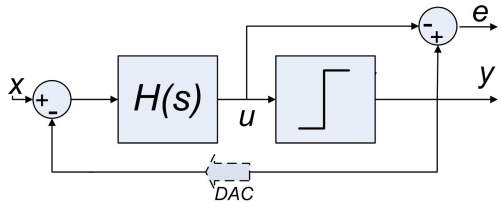

Figure 4. Block diagram of a ΣΔ modulator.

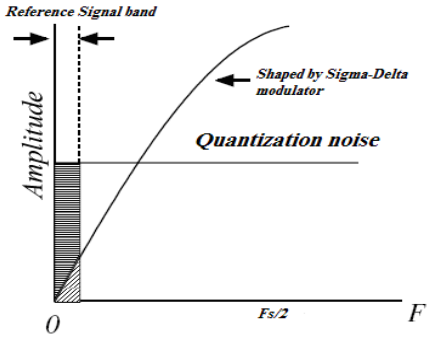

Figure 5. The ΣΔ modulator noise shaping characteristic.

Fig. 6 shows a multilevel ΣΔ modulation control. A multilevel ΣΔ modulator generates multi-bit data stream. Decoding the output of the multilevel ΣΔ modulator yields several different output states which can subsequently be used to control the on/off states of the switches in the inverter. Modulator design task requires selection of amplifier gain, the saturation limits of the integrator, and the sampling frequency and threshold of the hystersis loop. Tracking characteristics of the synthesized output voltage depends on the appropriate selection of the above mentioned parameters.

A. *Current control*

Fig. 3 shows the schematic diagram of a three-phase five-level FCMLI utilized in a shunt APF. V_c is the DC link of inverter and C_5, C_4, C_3, which are regulated using control scheme at $3V_c/4$, $V_c/2$, $V_c/4$ respectively.

TABLE I lists the switch combinations used in to the output phase voltage van with respect to n. The state "1" and "0" indicate the corresponding switch is on and off, respectively. TABLE I also indicates the state of flying capacitor "+", "-" and "N" indicate charging, discharging and no charging/discharging respectively for positive direction of current waveform (outgoing). The capacitor states will reverse for the negative current. The detailed operation and structure details of FCMLI can be found in [10].

In proposed control, first stage of ΣΔ modulator determines output voltage level of inverter with respect to compensating current error by a digital number. If reference current alters rapidly, the quantizer output may skip of one or several levels. Transition of the voltage level in this case will be by two levels or more. This will deteriorate the output voltage waveform and the advantages of the multilevel inverters will be lost. So by encumbering quantizer to mutate sequentially, the voltage level transition is step by step and uniformity in change in output voltage states occurs.

B. *Flying capacitor voltage control*

Flying capacitor voltage balancing under ΣΔ modulation control can be achieved using the redundant switching combinations available for different voltage level outputs (TABLE I) [10].

Each error between the actual flying capacitor voltages (v_{c3}, v_{c4}, v_{c5}) and their corresponding reference values are passed through a hystersis band comparator, individually. The output of each comparator is sampled at a constant frequency. At a particular sampling instant if the flying capacitor voltage error is positive, then that particular capacitor is required to be discharged; if it is negative, then charging is required and if error is in hystersis band, then no change in flying capacitor voltages is required. Therefore the desired operation for each flying capacitor is set. Now based on the desired output voltage level which is calculated by current control section, the direction of compensating current and the desired flying capacitor voltage operations at a particular instant, a particular switch combination is chosen form TABLE I by MLILI so that it can result in the desired output current and flying capacitor voltages.

There may be the case when not all the capacitors are involved in particular switching combination, as it evidence from TABLE I. in that case, that particular combination will be chosen which offers most favorable situation for flying capacitors that causes some deregulation in voltage of some of the flying capacitors. Besides sampling frequency and hystersis band of comparator determine voltage tolerance, so if charging interval is too large and/or hystersis band of comparator is too wide, it will deteriorate the output voltage waveform. This is because, the combined flying capacitor voltages will significantly add or subtract to the DC link voltage depending on the current path and will therefore affect the output voltage waveform. To overcome to this problem, the power stage of converter is embedded in the ΣΔ loop in proposed system. Therefore, the divisional voltage deregulation is part of the quantization noise and will be attenuated by ΣΔ loop. By this way, output of MLFCI is insensitive to divisional voltage deregulation.

TABLE I. SWITCHING SCHEME FOR ONE-PHASE LEG OF A 5-LEVEL FCMI

S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}	S_{18}	C_5	C_4	C_3	V_{an}
1	1	1	1	0	0	0	0	N	N	N	$+V_{DC}/2$
1	1	1	0	1	0	0	0	N	N	+	$+V_{DC}/4$
1	1	0	1	0	1	0	0	N	+	-	
1	0	1	1	0	0	1	0	+	-	N	
0	1	1	1	0	0	0	1	-	N	N	
0	0	1	1	0	0	1	1	N	-	N	0
0	1	0	1	0	1	0	1	-	+	-	
0	1	1	0	1	0	0	1	-	N	+	
1	0	0	1	0	1	1	0	+	N	-	
1	0	1	0	1	0	1	0	+	-	+	
1	1	0	0	1	1	0	0	N	+	N	
1	0	0	0	1	1	1	0	+	N	N	$-V_{DC}/4$
0	1	0	0	1	1	0	1	-	+	N	
0	0	1	0	1	0	1	1	N	-	+	
0	0	0	1	0	1	1	1	N	N	-	
0	0	0	0	1	1	1	1	N	N	N	$-V_{DC}/2$

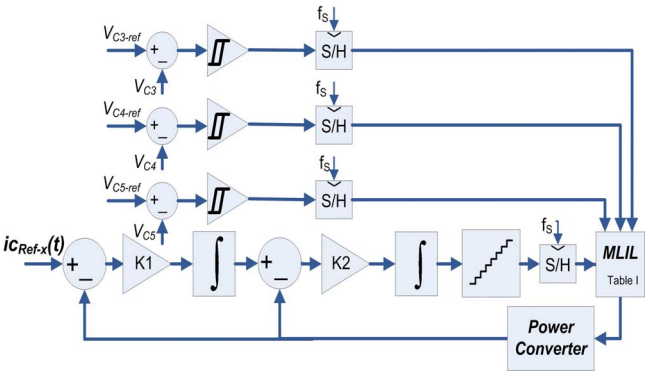

Figure 6. Control block diagram of one phase of a 5-level FCMLI.

V. SIMULATION RESULTS

Fig. 3 has shown the topology of a shunt APF based on five-level flying capacitor inverter. The nonlinear load is represented by a transformer front-end 3-phase thyristor controlled rectifier supplying an R-L load. The APF is connected to grid through a filter featured L_f-R_f. this is necessary to eliminating current ripple due to switching. The parameter values for system indicated in TABLE II.

Load current i_L and AC mains voltage v_a are shown in Fig. 7. Note that simulations is made for three-phase system, but just one phase (Phase a) is shown in figures to make images clear to hinder of visual error. It shows source current before filtering are distorted and are not in phase with the source voltage.

The source voltage; compensated line current and filter current of proposed system are illustrated also in Fig.7. It is evidence from Fig. 7 that presented system is capable to compensate harmonic and reactive current perfectly and makes system current in phase with system voltage without any considerable harmonic.

Fig. 8 shows system performance and capability at DC link and flying capacitor voltages regulation.

TABLE III shows the general characteristics of system in term of power factor and harmonic components that confirms system has satisfactory performance.

TABLE II. PARAMETER VALUES OF SIMULATION

Parameter		**Parameter value**
System Voltage / Frequency		6.6 $kV_{L\text{-}L}$ / 50Hz
Load		3-Phase thyristor rectifier with 20° firing angle with 15 Ohm resistant load, fed by a YΔ transformer
Passive Filter	L_f	0.6mH
	R_f	0.2Ω
DC link Capacitors	C_1	1200μF
	C_5	470μF
	C_4	330μF
	C_3	150μF
DC link reference voltage		5.5kV
Sampling frequency		10 kHz

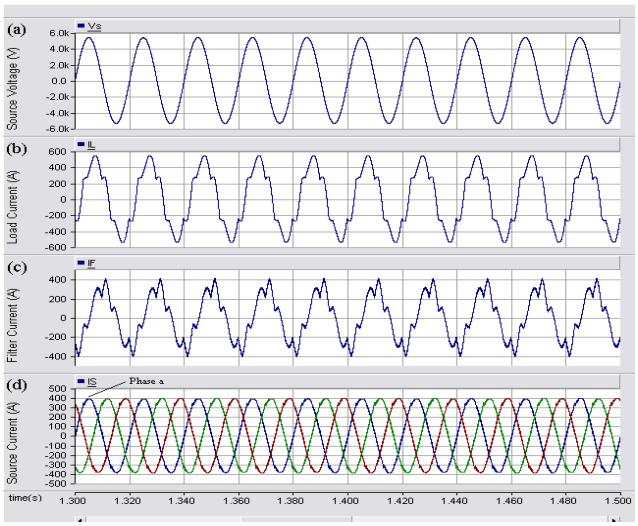

Figure 7. Simulation results (phase a); (a) Main voltage; (b) Load current; (c) Filter current; and (d) system currents.

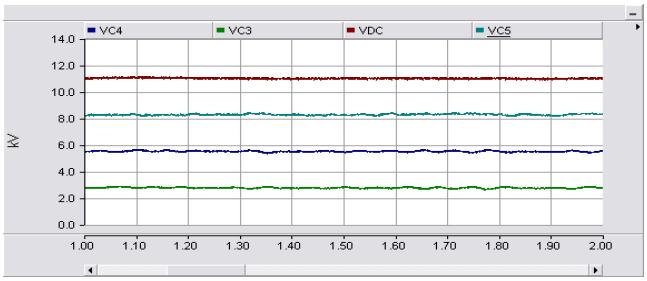

Figure 8. DC link and phase a flying capacitor voltages.

TABLE III. HARMONIC COMPONENTS DEMANDED TO AC MAINS BY A NON-LINEAR LOAD WITH PROPOSED APF (AS A PERCENT OF THE FUNDAMENTAL)

	Without AF	***Sigma-Delta controlled AF***
PF	0.819	0.999
I_3	0.01%	0.2%
I_5	18.55%	1.2%
I_7	6.86%	0.25%
I_9	≈0%	0.06%
I_{11}	1.87%	0.43%
I_{13}	1.68%	0.33%
I_{15}	≈0%	0.12%
I_{17}	1.31%	0.41%
I_{19}	0.58%	0.18%
THD	20.02%	1.6%

VI. CONCLUSION

This work presents a ΣΔ modulated flying capacitor multilevel inverter based shunt active power filter. In control section of this APF, reference currents are generated by PHC method, which has guaranteed performance under any condition of use. Use of a multilevel inverter makes possible direct connection of the APF to the increased voltage network. Besides, APF profits from FCMLI other advantages such as flexibility, lower electromagnetic interference (EMI), higher efficiency, lower device switching and suppression of offensive harmonics which generate by APF itself.

To enhance APF performance further, 2nd-order ΣΔ modulation control is used to control FCMLI. This modulator shapes in band noise to higher frequencies, so allows a significant reduction of the filtering requirements. In addition, it reduces EMI further, and omits complicated PWM control. Furthermore to reduce flying capacitor voltage deregulation and system nonlinearity power section of APF is embedded in ΣΔ control loop that causes more improvement of APF performance.

Simulation results verified that this APF can compensate the harmonic currents and reactive power correctly and better.

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